REMARKS

The above amendments to the above-captioned application along with the following remarks are being submitted as a full and complete response to the Office Action dated April 2, 2003 (U.S. Patent Office Paper No. 8). In view of the above amendments and the following remarks, the Examiner is respectfully requested to give due reconsideration to this application, to indicate the allowability of the claims, and to pass this case to issue.

Status of the Claims

As outlined above, claims 18 - 27 are being canceled without prejudice or disclaimer. Claims 1 - 17 and 28 - 37 stand withdrawn from consideration in this application. In addition, new claims 38 through 42 are hereby submitted for consideration.

Prior Art Rejections

Claims 18, 19, 21, 23, 24, and 25 were rejected under 35 U.S.C. §102(b) allegedly being anticipated by Tadashi, Japanese Publication No. 11-111,845. Applicants respectfully traverse this rejection.

The Examiner, on page 2, line 17 – page 3, line 9 makes reference to Fig. 3B, Fig. 3D, Fig. 3E and page 4, lines 24-33 as being anticipatory to the subject matter disclosed by the above referenced claims.

Applicants carefully reviewed the figures and the section referenced and would like to respectfully draw the Examiner's attention to paragraph [0050] of the Tadashi reference, that recites: "by passing through the process which gave drawings 3(d) – (f) explanation of the 1st operation gestalt, the semiconductor device shown in drawing 6 is formed."

Referring to the device illustrated in Fig. 6, Applicants observe that it discloses an embedded wiring with a W via , that has capping layers to prevent the outer moisture from reacting with the lower fluorine –containing silicon oxide film.

Applicants carefully reviewed the Tadashi reference and noticed that the reference does not disclose or makes reference to a dual-damascene method. The reference further makes no reference to embedded copper wiring.

In contrast, the present invention discloses a fabrication method of integrated cir[redacted] having copper wiring of dual damascene type, where the Young modulus of an in[redacted] portion of the interlayer dielectric film is such that stress mi[redacted]

The dual damascene structure of the present invention presents an inter-via layer portion of SiOF and an inter-wiring layer portion. An embedded copper via is present in both layer portions. An upper later dielectric film of SiO2 is deposited as part of the inter-wiring layer portion but not as part of the embedded via, pertaining to the copper via. An inter-layer dielectric fill is also present.

In contrast, the device disclosed by the Tadashi reference presents a lower layer dielectric film of SiOF, an SiN layer and an upper layer dielectric film of SiO2. Through all 3 layers an embedded via topped by an embedded wiring is present. An inter-layer dielectric fill is present.

In view of the differences outlined above, Applicants respectfully request the Examiner to reconsider the pending claims. Due to the above exhibited differences, the Tadashi reference does not anticipate the pending claims. Therefore, the Examiner is respectfully asked to withdraw the rejection and to pass the claims to issue.

Claims 20, 22, and 26 were rejected under 35 U.S. C.§103(a) as allegedly being unpatentable over Tadashi in view of Wolf. Applicants again respectfully traverse.

Applicants have reviewed the Wolf reference The reference regarding copper in the Wolf document on page 193, paragraph 2 is made in the context where "copper thin films offer even low resistivity (1.7 μΩ-cm) than Au films, and they are also expected to show good electromigration resistance. They would thus appear to be attractive VLSI conductor materials, especially as device dimensions approach deep-submicron sizes. A dry-etching process for Cu films has not been successfully developed (see Vol. 1, chap. 16), however, and this is one of the chief reasons that Cu has not been widely considered for such applications."

Applicants will contend that the Wolf document only discloses that Cu thin films are referred to as an alternative to Au films. Specifically, on page 192-4, referred to by the Examiner in the office action on page 4, paragraph 2, Wolf refers to copper wiring as an alternative for conventional Al wiring.

Neither Tadashi nor Wolf separately or in combination discloses all the features of the pending claims. Therefore, these references do not anticipate or render obvious the subject matter disclosed by the above referenced claims. Applicants respectfully ask the Examiner to reconsider all the pending claims and pass this case to issue.

CONCLUSION

In view of all the above, Applicants respectfully submit that certain clear and distinct differences as discussed exist between the present invention as now claimed and the prior art

references upon which the rejections in the Office Action rely. These differences are more than sufficient that the present invention as now claimed would not have been anticipated nor rendered obvious given the prior art. Rather, the present invention as a whole is distinguishable, and thereby allowable over the prior art.

Favorable reconsideration of this application as amended is respectfully solicited. Should there be any outstanding issues requiring discussion that would further the prosecution and allowance of the above-captioned application, the Examiner is invited to contact the Applicant's undersigned representative at the address and phone number indicated below.

Respectfully submitted,

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